CLAIM AMENDMENTS

1. (currently amended) A method for enabling a stand-alone integrated circuit (IC), the method comprises the steps of:

a) establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

b) receiving a power enable signal;

c) enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source, wherein the enabling includes:

generating a clock signal;

generating power converter regulation signals based on the clock signal;

enabling a band-gap reference that is used in generating the power converter regulation signals; and

d) when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.

2. (original) The method of claim 1, wherein the establishing the idle state further comprises enabling a reset signal for the at least a portion of the stand-alone IC.

3. (original) The method of claim 2, wherein the establishing the idle state further comprises generating a clock signal.

4. (original) The method of claim 3, wherein the enabling of the functionality of the stand-alone IC further comprises providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

5. (canceled)

6. (canceled)

7. (original) The method of claim 1 further comprises generating a clock lock signal when the clock has substantially reached a substantially steady-state.

8. (original) The method of claim 7, wherein the enabling functionality of the stand-alone IC further comprises:

detecting the clock lock signal; and

detecting a supply lock signal; and

de-asserting a reset signal upon detection of the clock lock signal and the power supply lock signal.

9. (original) The method of claim 1, wherein the enabling the on-chip converter further comprises:

generating a first supply from the power source; and

generating a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

10. (original) A stand-alone integrated circuit (IC) comprises:

a reset circuit operable to place the stand-alone IC in an idle state until a supply lock signal is enabled;

an on-chip power converter that generates a supply from an external power source upon assertion of a power enable signal; and

supply lock circuit operably coupled to enable the supply lock signal when the supply substantially reaches a steady-state condition.

11. (original) The stand-alone IC of claim 10, wherein the reset circuit further comprises:

clock generator operably coupled to produce a clock signal when the external power source is coupled to the stand-alone IC, wherein the clock signal is provided to the on-chip power converter such that the on-chip power converter generates the supply;

clock lock module operably coupled to generate a clock lock signal when the clock signal has substantially reached a steady-state condition;

reset module operably coupled to assert a reset signal when the external power source is coupled to the stand-alone IC, wherein the reset module de-asserts the reset signal when the clock lock signal and the supply lock signal are

asserted such that functionality of the stand-alone IC is enabled.

12. (original) The stand-alone IC of claim 9, wherein the on-chip power converter further comprises:

a band-gap reference that produces a reference voltage upon assertion of the power enable signal.

13. (original) The stand-alone IC of claim 9, wherein the on-chip power converter further comprises:

switching transistors operably coupled to produce a first supply and a second supply from the external power source and a single inductor, and

regulation module operably coupled to the switching transistors, wherein the regulation module produces control signals that enable and disable transistors of the switching transistors to regulate the first and second supplies.

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14. (original) A stand-alone IC comprises:

on-chip power converter;

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

establish an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

receive a power enable signal;

enable, in response to the power enable signal, the on-chip power converter of the stand-alone IC to generate at least one supply from the power source; and

when the at least one supply has substantially reached a steady-state condition, enable functionality of the stand-alone IC.

15. (original) The stand-alone IC of claim 13, wherein the memory further comprises operational instructions that cause the processing module to establish the idle state by enabling a reset signal for the at least a portion of the stand-alone IC.

16. (original) The method of claim 2, wherein the establishing the idle state further comprises generating a clock signal.

17. (original) The stand-alone IC of claim 15, wherein the memory further comprises operational instructions that cause the processing module to enable the functionality of the stand-alone IC by providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

18. (original) The stand-alone IC of claim 14, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by:

generating a clock signal; and

generating power converter regulation signals based on the clock signal.

19. (original) The stand-alone IC of claim 18, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by enabling a band-gap reference that is used in generating the power converter regulation signals.

20. (original) The stand-alone IC of claim 18, wherein the memory further comprises operational instructions that cause the processing module to generate a clock lock signal when the clock has substantially reached a substantially steady-state.

21. (original) The stand-alone IC of claim 20, wherein the memory further comprises operational instructions that cause the processing module to enable functionality of the stand-alone IC further comprises:

detect the clock lock signal; and

detect a supply lock signal; and

de-assert a reset signal upon detection of the clock lock signal and the power supply lock signal.

22. (original) The stand-alone IC of claim 14, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip converter further comprises:

generate a first supply from the power source; and

generate a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.